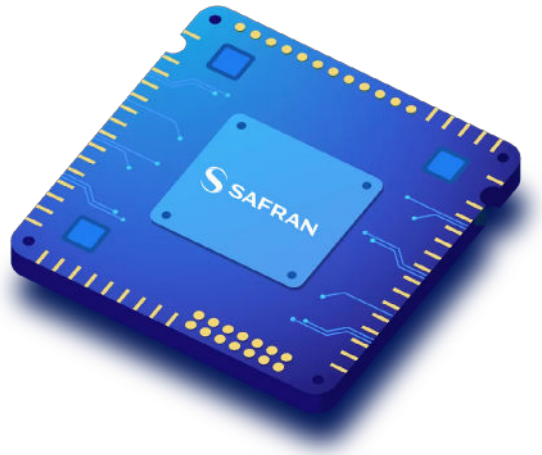
ELECTRONICS & DEFENSE

HATI

High Accuracy Timing IP



HATI v2.2

The HATI (High Accuracy Timing IP) is a FPGA core designed to provide sub-nanosecond synchronization accuracy by using 1 Gbps optical fiber links.
It works as a White Rabbit (WR) slave node implemented on the FPGA, using a Safran's WR-Z device as master.
The IP core is based on precise internal clock corrections to achieve sub-nanosecond synchronization accuracy and stable frequency dissemination. Its architecture allows to adapt the IP to different platforms.
The HATI IP Core contains the whole design from the transceiver to the FPGA logic, and embeds a soft processor for easy configuration and management. All the required clocking circuitry to achieve a highly accurate synchronization is implemented using only FPGA resources.

- Sub-nanosecond time accuracy over 1Gbps Ethernet optical fiber interfaces using WR.
- Easy deployment: plug & play solution over 10 km using optical fiber links without need of link calibration.
- Dynamic compensation of asymmetries caused by weather conditions.
- High-accurate and deterministic timing integration on the FPGA.
- No need for expensive oscillators/clocks or dedicated hardware.
- Optimized FPGA resources utilization.

Safran Electronics & Defense is with you every step of the way, building in the intelligence that gives you a critical advantage in observation, decision-making and guidance.

SAFRAN

HATI Description

HATI implements the White-Rabbit protocol (basis of the IEEE-1588-2019 High Accuracy) in slave mode to provide sub-nanosecond timing transfer over optical fiber links to FPGA devices requiring just optical Ethernet interfaces. HATI allows to distribute not only sub-nanosecond time but also stable frequency reference over the same link.

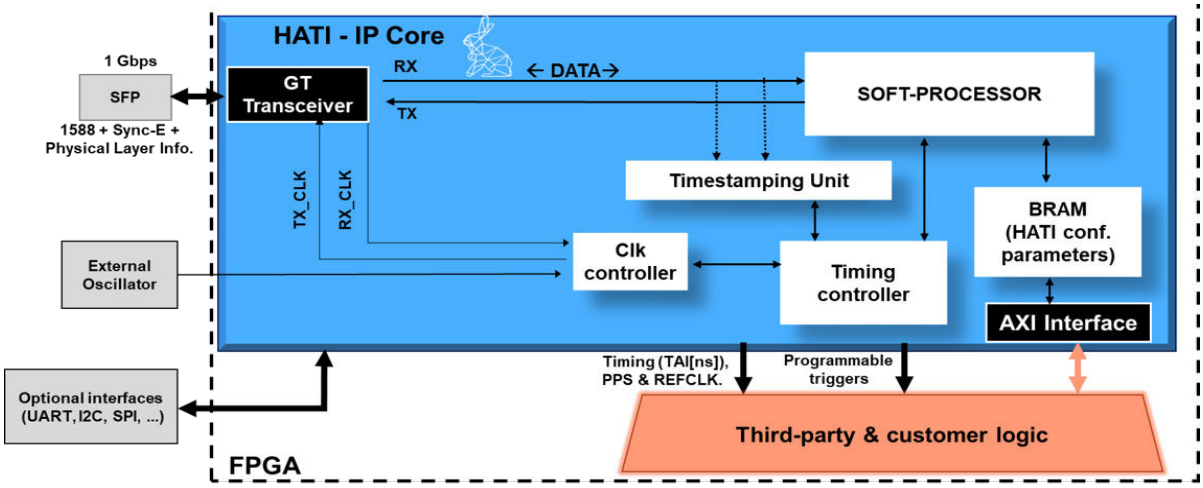
HATI is provided as a Xilinx FPGA IP core for customer integration or as an integrated feature in third-party partners' network devices.

It includes AXI interface for management and monitoring from the user logic. It also brings optional interfaces as UARTs or SPI/I2C interfaces to allows configuration or calibration parameters non-volatile storage, reading IP status, etc. No CPU is required for operation although it is recommended for management.

HW Requirements to support HATI

- The HATI must be physically connected to an SFP cage outside the FPGA.
- The HATI core needs a 125 MHz clock from an external source.
- One general purpose FPGA pin must be directly connected to some external coaxial connector (SMA or equivalent) for calibration.
- One time calibration is needed when a new HATI FPGA binary is generated.
- It's recommended to use the HATI along with a hard-processor (Zynq SoCs or external ARMs) for operation.
- Available FPGA resources (see table).

HATI stand-alone FPGA block design



Supported tools devices

- Vivado 2019.x, 2020.x.

Supported FPGA families:

- Kintex7, Kintex7-US, Kintex-7US+, Artix-US+, Virtex7 & Virtex7-US+, Zynq, Zynq-US+.

Contact us for other versions or platforms.

HATI FPGA interface and resources (Xilinx XC7Z035FFG900-2)

Resource	Used	Available	Utilization %
LUT	14404	171900	8.38%
Registers	14102	343800	4.1%
BRAM	82	500	16.4%
DSP	6	900	0.67%
MMCM	2	8	25%
PLL	2	8	25%

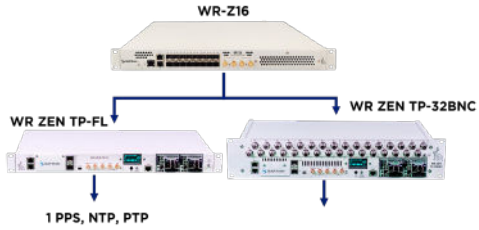
HATI: Implementation Guide

I need to create a WR end node

A WR end node is a WR slave which gets its time from WRZ device and locally redistributes time in other formats like 1PPS, NTP, PTP, etc.

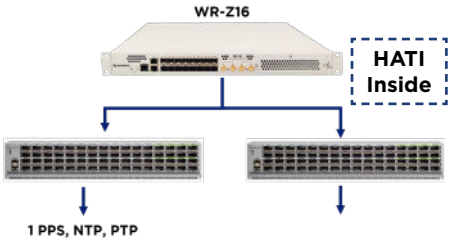
- There is room in my network to add WR standard HW products, which embed full WR protocol, plus power management, monitoring, security, etc.
- I need only a small number of end nodes in my network.
- I don't have the resource or skills to embed a WR stack in a FPGA (this is really complex...) and prefer to focus on my operations.

Consider using COTS standalone WR appliances:
- WR-Z16
- WR ZEN TP-FL
- WR ZEN TP-32 BNC



- There is limited room in my network to add WR standard HW products and will appreciate that some standard network elements embed this WR end node capability.
- I need a high number of WR end nodes.
- I don't have the resource or skills to embed a WR stack in a FPGA (this is really complex...) and prefer to focus on my operations.

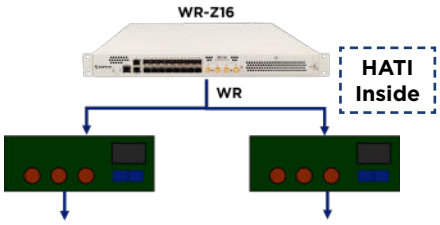
Consider using WR HATI enabled routers/switches, like ARISTA 7130 LB



3d party HATI enabled router/swtich

- There is limited room in my network to add WR standard HW products or I have specific HW for harsh environment, or security, or other reasons, that requires WR capability.
- I need a high number of WR end nodes.
- I have the resource and skills to embed an WR stack based on an IP core in a FPGA.

Consider creating your own HATI enabled device, by integrating HATI in your FPGA



Your own HATI enabled HW device

Offer structure

Using 3rd party HATI enabled network elements

Customer will receive the file for the license activation of the HATI in the WR-Z master device. This allows to establish a WR link between the WRZ master device and the third-party HATI enabled device.

Offer elements:

- WRZ device (master WR node).
- WR HATI Activation permanent license (per port) -Tied to WR-Z device
- WR Support contract for the WR-Z device.

Using your custom FPGA board.

An integration project is required for the HATI integration. Customer will receive the HATI, integration support and the necessary documentation to ensure the successful integration of the HATI in their customer node.

Offer elements:

- HATICORE-1000 - Tied to your own device (includes HATI provision and HATI integration support)
- WRZ device (master WR node)
- WR HATI permanent activation license (per port) - Tied to WR-Z device
- HATICORE yearly support (including fw updates)
- Optional customization for HATICORE implementation.
- Optional customization for HATICORE support
- HATI Starting kit with WR-Z16 (optional)

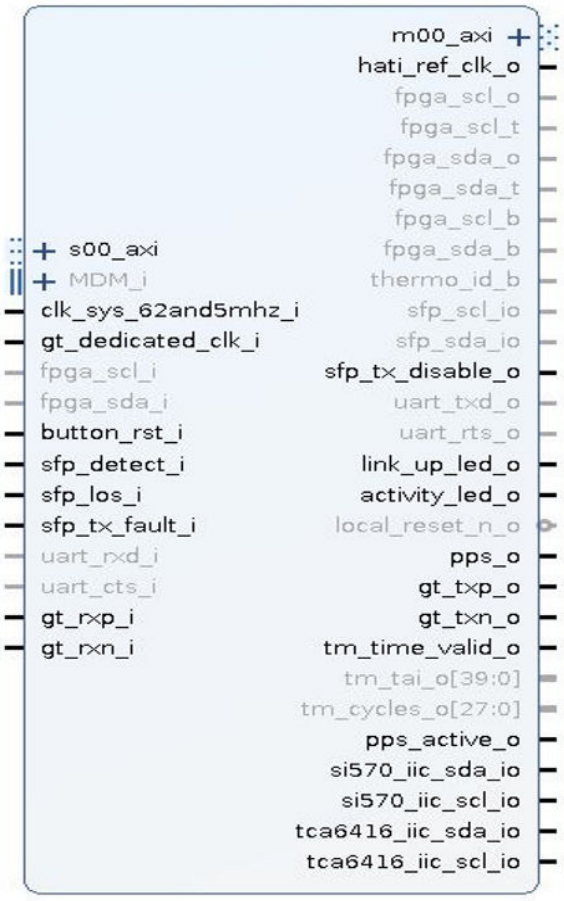
HATI: Interfaces and performance

HATI IP core interfaces

HATI can be integrated into Xilinx designs using Vivado tools (IP integrator of HDL files).

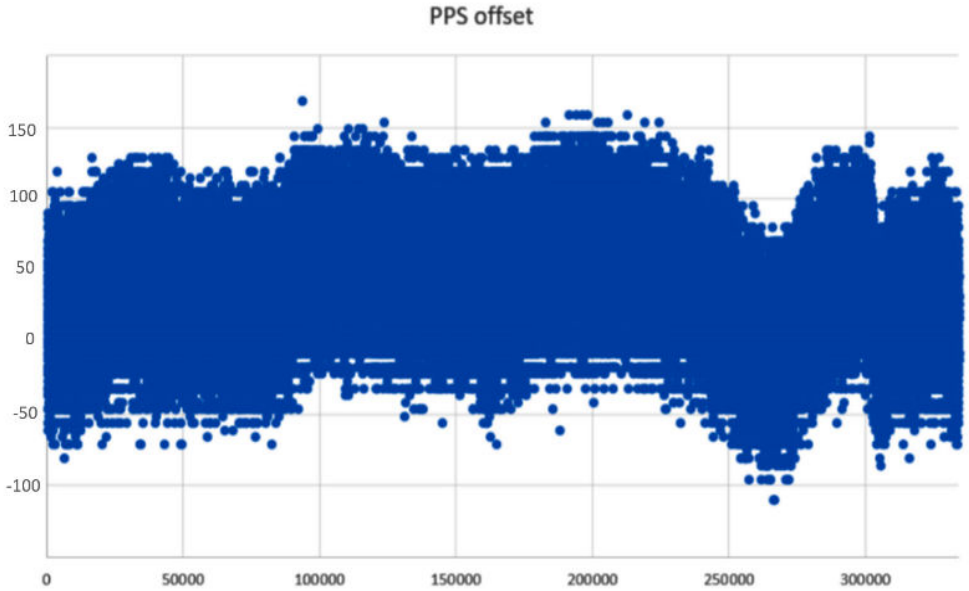
Main interfaces include:

- Clock input.
- GT and SFP signals.
- AXI connection for management and monitoring.
- Timing outputs (1PPS, 62,5 MHz frequency reference and internal 16 ns TAI counters).
- Optional interfaces for UART, I2C or SPI connections.



Performance

The figure on the right shows the level of accuracy that can be achieved with HATI, measured by comparing the 1PPS (Pulse Per Second), outputs from a master WR-Z16 device and an FPGA board that integrates the HATI core working as a WR slave.
The obtained time error is less than +/- 150 picoseconds with a standard deviation of 43.15ps It is a long-term measurement using a short fiber cable to implement the WR link.



Peak to peak TE (ps).....280.66
Mean (ps).....52.54
Std. Dev. (ps).....43.15

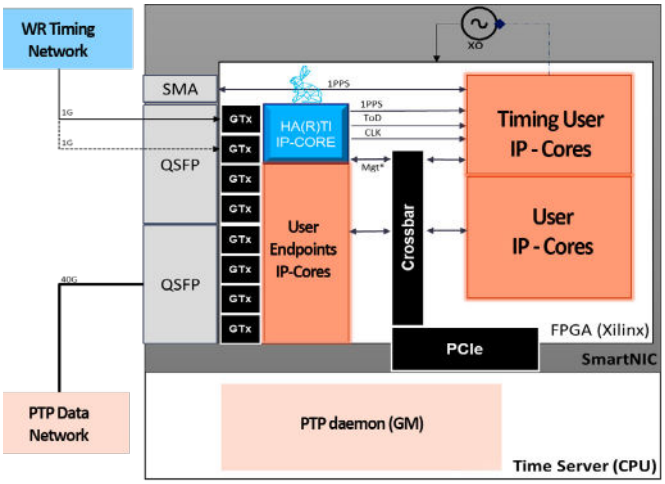
Use cases & purchase information

Use cases and applications in timing infrastructures:

HATI typical applications include its integration into distributed systems of sensors such as Radar, and other communications systems for Defense applications; synchronization of the timestamping devices of the capture network for Finance; and improved datacenter server synchronization thanks to NICs integration, providing deterministic time error and minimal impact on timing performance due of the network topology or data traffic.

Example: HATI time base for timestamping

Example: HATI enabled SmartNIC

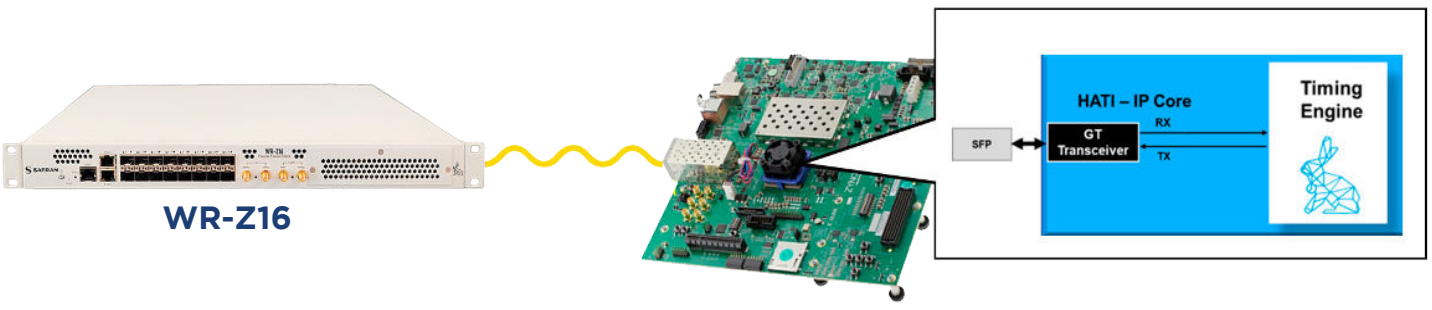


HATI starting kit

A starting kit is available for customers interested in evaluating the HATI and exploring the possibility of integrating the HATI into their own hardware. This kit includes all the necessary elements to build a simple plug & play WR setup based on HATI.

HATI starting kit BOM

- 1x Xilinx ZCU102 with HATI enabled (includes PMOD to 2xSMA adapter)
- 1x WR-Z16
- 1x HATI activation license
- User guide
- 1xLC-LC optical fiber (2m)
- 4x SMA-BNC coaxial cables
- 1x pair of SFPs



WR-Z16

Xilinx ZCU102

POWERED BY TRUST

safran-navigation-timing.com

SAFRAN

July 26, 2023