TPRO-PMC/TSAT-PMC
SYNCHRONIZABLE TIMECODE GENERATOR with PMC BUS INTERFACE

User Manual

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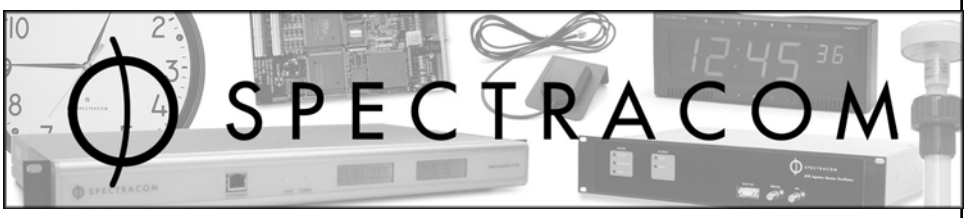

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THE ANALOG CLOCKS ARE WARRANTED FOR ONE YEAR FROM DATE OF SHIPMENT AND SUBJECT TO THE EXCEPTIONS LISTED ABOVE.

THE TIMECODE READER/GENERATORS ARE WARRANTED FOR ONE YEAR FROM DATE OF SHIPMENT AND SUBJECT TO THE EXCEPTIONS LISTED ABOVE.

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Spectracom products must be returned with the description of the claimed defect and identification of the individual to be contacted if additional information is needed. Spectracom products must be returned properly packed with transportation charges prepaid.

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Extended warranties can be purchased for additional periods beyond the standard five-year warranty. Contact Spectracom no later than the last year of the standard five-year warranty for extended coverage.

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1 Overview

The TPRO-PMC and TSAT-PMC provide high-accuracy timing functions on a plug-in board for the PMC computer bus. The board has an on-board clock, which is kept in sync to either an external timecode input (TPRO-PMC) or to time provided by the GPS satellites (TSAT-PMC). Several timing functions are derived from the on-board clock, including a programmable periodic pulse rate output ("Heartbeat"), a programmable start/stop output ("Match"), a selectable frequency output ("Oscillator Out", 1 kHz, 1, 5, or 10 MHz), and a time-stamping input ("Time-Tag").

The TSAT-PMC includes an externally mounted GPS antenna and a 100-foot cable to connect the antenna to the board. The GPS satellites provide continuous time and position information, available anywhere in the world. It automatically syncs its on-board clock to the time transmitted by the GPS satellites and disciplines the onboard 10 MHz oscillator to maintain a 1 microsecond accuracy. The board outputs a timecode signal, in IRIG-B format, which conveys the day, hour, minute, and second. It also has a 1 kHz carrier referenced to the on-board oscillator.

The TPRO-PMC is similar to the TSAT-PMC, except it obtains time from an input timecode. The timecode can be in IRIG-A, IRIG-B, or NASA36 format. The board automatically detects which format is being used. The timecode conveys the day, hour, minute, and second. The on-board 10 MHz oscillator is disciplined to maintain an accuracy of 10 microseconds for IRIG-A and 15 microseconds for IRIG-B and NASA36.

Either board may be used as a stand-alone timecode generator. The computer programs the day, hour, minute, and second. The board then continues to count from that time, using the on-board oscillator as the timebase reference. This is called "freewheeling."

The host computer communicates to either board through a set of memory-mapped registers. When the computer boots up, the board identifies itself to the PMC bus by specifying the unique Subsystem Vendor ID and Subsystem Device ID. The host computer can then read the instantaneous time, and command the board to set time, and/or to provide an interrupt at a periodic rate, at a specified time, and/or when a time-tag event occurs.

Front panel indicator lights indicate when the board is in the process of synchronizing ("acquiring") the GPS or timecode input signal and when the board has established valid synchronization. The host computer can also interrogate the status register to determine these and other conditions.

1.1 General Information about GPS

NOTE: GPS applies only to the TSAT-PMC board; the TPRO-PMC is not equipped for GPS.

The United States government operates a set of approximately 32 satellites, collectively known as the "GPS Constellation" or "GPS Satellites." Each satellite has an internal atomic clock and transmits a signal specifying the time and satellite position. On the ground, the GPS receiver determines its position (longitude, latitude, and elevation) and the time by decoding the signals simultaneously from at least four of the GPS satellites.

The satellite orbits are circular, inclined approximately 56 degrees from the equator, orbiting the Earth once every 11 hours. There are several different orbital planes providing continuous coverage to all places on Earth. The GPS receiver uses an omni-directional antenna; the satellites move slowly across the sky (they are not at fixed locations).

Each satellite transmits a spread-spectrum signal, centered at 1575.42 MHz. When power is first applied, the GPS receiver begins searching for the satellites. It does this by searching for each satellite individually, listening for each satellite's distinct spread-spectrum hopping sequence. This process can take a few minutes, as the receiver iteratively locates satellites, refines its position, and determines for which satellites to search.

The GPS receiver retains the last known position when the power is switched off. This results in faster satellite acquisition the next time the receiver is switched on. If the antenna has been moved more than a few miles, however, acquisition time will be slightly longer, as it must first re-compute the position.

1.2 Your Spectracom GPS Receiver

Your board's GPS receiver is built into the antenna housing and communicates to the board via a serial (RS-422) interface. Power (+12V) is supplied from the board. The unit comes with a 100-foot cable. Extension cables are available in 100-foot lengths. The maximum total length is 500 feet. The connectors on the extension cables are not weatherproof; only the first 100-feet can be outdoors. The cable consists of several twisted pairs (not coaxial cable) and a foil shield.

NOTE: Spectracom recommends applying an appropriate silcon grease to the cable connection at the GPS antenna in order to protect the connection from moisture. An additional weatherproofing kit (P/N 221213) containing butyl rubber and plastic tape is also available from Andrews Corporation, US 800.255.1479.

1.3 Inventory

Before installing the board, please verify that all material ordered has been received. If there is a discrepancy, please contact Spectracom Customer Service at US 585.321.5800.

Item	Quantity	Description
1	1	Operation & Maintenance Manual
2	1	Board
3	1	Breakout Cable (micro DB-25 to several BNC connectors)
4	1	GPS Receiver/Antenna (TSAT-PMC only)
5	1	100-foot Antenna Cable (TSAT-PMC only)

1.4 Inspection and Support

Unpack the equipment and inspect it for damage. If any equipment has been damaged in transit, please contact Spectracom Customer Service at US 585.321.5800.

If any problems occur during installation and configuration of your Spectracom product, please contact Spectracom Technical Support at US 585.321.5823 or US 585.321.5824.

CAUTION:  *Electronic equipment is sensitive to Electrostatic Discharge (ESD). Observe all ESD precautions and safeguards when handling the timecode generator.*

NOTE: If equipment is returned to Spectracom, it must be shipped in its original packing material. Save all packaging material for this purpose.

1.5 External Connections

Only those functions that are actually used need to be connected. Always switch off the computer's power before connecting or disconnecting.

1.6 GPS Antenna Connector (TSAT-PMC Only)

The TSAT-PMC has a commercial Micro–D 15 pin plug connector that connects to the GPS antenna via the supplied cable. The supplied cable and the optional extension cable include shielding to meet EMI requirements. Use of other cables is not recommended. The optional extension cable is for indoor use only.

When power is first applied, the board sends initialization commands to the receiver/antenna. For this reason, do not disconnect and reconnect the antenna while power is applied.

1.7 Timing Connector

Both the TPRO-PMC and TSAT-PMC have a 25 pin commercial Micro–D receptacle (timing) connector. The pinout of this connector is the same for both TPRO-PMC and TSAT-PMC:

Pin	Function	Type
1	1-PPS+	Differential Output
2	1-PPS-	Differential Output
3	Match	TTL Output
4	Antenna 1-PPS	TTL Output (active only with TSAT-PMC)
5	Heartbeat	TTL Output
6	Disciplined Oscillator +	Differential Output
7	Disciplined Oscillator -	Differential Output
8	Application Specific 3	TTL Output
9	Application Specific 4	TTL Input
10	IRIG-B	Analog Output
11	Application Specific 6	TTL Input
12	Timecode IN+	Differential Analog Input
13	Timecode IN-	Differential Analog Input
14	Application Specific 0	TTL Output
15	GND	--
16	Time Tag External Event	TTL Input
17	Sync Indicator	Open Collector Output
18	Application Specific 1	TTL Output
19	GND	--
20	Application Specific 2	TTL Output
21	GND	--
22	Application Specific 5	TTL Input
23	GND	--
24	Application Specific 7	TTL Input
25	GND	--

A 15-pin Micro-D connector, GPS Antenna Connector P2, is provided with the TSAT-PMC only. The pinout of this connector is as follows:

Pin	Function	Type
1	UP+	Differential Output
2	UP-	Differential Output
3	no connect	--
4	1-PPS+	Differential Input
5	1-PPS-	Differential Input
6	no connect	--
7	GND	--
8	+12 V	Supply Output
9	+12 V	Supply Output
10	GND	--
11	DOWN+	Differential Input
12	DOWN-	Differential Input
13	no connect	--
14	GND	--
15	no connect	--

1.8 Breakout Cable

A breakout cable assembly is supplied with each board to permit access to the most commonly used features. This cable consists of a 25-pin plug and five BNC sockets.

The breakout cable for standard boards uses a shorter cable for the Timecode Input than for the other signals. This is because the Timecode Input is a differential signal; the shield (Timecode Input-) is not connected to Signal Ground on the board. The shorter cable prevents the shield from touching the other shields, thus preserving the isolation from Signal Ground. (In most applications, the Timecode Input- is connected to Signal Ground on the user's end.)

1.9 Timecode Input

This differential analog signal consists of an amplitude-modulated sine wave. It can be IRIG-A, IRIG-B, or NASA36 format. The board automatically detects the format and establishes synchronization. No commands need to be sent from the host computer to establish synchronization.

NOTE: The IRIG-A format is 132. The IRIG-B format is 122 and does not support the control function or straight timing seconds fields.

The carrier frequency depends on the code format (1 kHz for IRIG-B and NASA36, 10 kHz for IRIG-A). IRIG-B is by far the most popular format. The sine wave has two distinct amplitudes, called mark and space. The ratio of mark:space is 3:1. An AGC circuit accommodates a wide range of possible input amplitudes, as described in the Specifications section.

Timecodes, regardless of format, convey the Julian day (001-366), hour, minute, and second. Precise frequency is also conveyed. The year and date are not conveyed. The board phase-locks and disciplines its on-board oscillator to the timecode carrier. This results in an accuracy of 10 microseconds for IRIG-A and 15 microseconds for IRIG-B and NASA36. (IRIG-A accuracy is slightly better than IRIG-B and NASA36 because IRIG-A has a faster/higher carrier frequency.)

Timecodes are essentially audio signals. They can be distributed by coax or twisted pairs for long distances (several hundred feet) without degradation. Cable and termination impedance is not critical, as the signal consists of a low-frequency sine wave. A single output can drive many (>10) inputs.

The timecode can be recorded on tape to time-stamp data, but there are several drawbacks to this. First, precision boards such as TPRO-PMC will not synchronize to a timecode being played back from tape, due to timebase flutter. Also, when recording, it is often necessary to reduce the amplitude of the signal. Otherwise, the recorder's AGC will compress the high and low parts to the same amplitude, losing the timing information.

Digitizing the timecode is not recommended, as the precise frequency information, contained in the carrier frequency, is lost. The board probably will not synchronize to a digitized reproduction of a timecode because of timebase errors.

1.10 Timecode Output

The board outputs an IRIG-B timecode signal capable of driving many (>10) boards.

The on-board clock generates the Timecode Output. It is always present. When the board is powered up, it begins counting from Day 001, hour 00, minute 00, second 00 (001:00:00:00). Valid Julian days range from 001 to 366. The invalid Julian day number (000) signifies that the clock has not been set. The Timecode Output will jump to the correct time when the clock is set (via the computer bus) or when synchronization is established with the Timecode Input (TPRO-PMC) or to GPS (TSAT-PMC).

There are two methods for using the Timecode Output to drive multiple boards' inputs. The "T" method connects the output of the master to each slave's input. The advantage of this is that, if any board loses the incoming signal, it will report a loss of sync and will not affect the other slaves. The disadvantage of this method is that an additional connector (usually a BNC "T") is needed at all but the master and last slave boards.

The other method is called "loop-through." The output of the master is connected to the input of the first slave. The output of the first slave is connected to the input of the second slave and so on. The advantage of this method is that no additional connectors are needed. If the signal is lost at a given board, however, all boards "downstream" from that board will have lost sync with the master. They will be in sync with each other (this is usually an advantage), but they cannot recognize or indicate loss of master sync (a disadvantage).

The user must determine which method is most suitable for the application. Most applications use the "T" method.

1.11 Time Tag Input

The board latches the on-board clock time into a holding register on the rising edge of this signal. The user's software is responsible for ensuring that each event is read before the next occurs.

This is a TTL input with an on-board 10K pull-up resistor to +5V.

1.12 1 PPS Output

This one pulse per second output comes from the on-board clock. It is present regardless of whether the board is synchronized or freewheeling. An RS-422 driver and series 10-ohm resistors in each line are on-board. The recommended termination is 120-ohms, ½ watt, line-to-line (not to ground). The 1PPS Output can be used as a single-ended TTL signal.

1.13 Oscillator Output

Software selects whether this signal is 10 MHz, 5 MHz, 1 MHz, 1 kHz, or Off. It is an RS-422 signal with 10-ohm resistors in each line on the board. The recommended termination is 120-ohms, ½ watt, line-to-line (not to ground). The driver is enabled (not tri-stated), held in the "zero" condition, when in the Off mode.

1.14 Heartbeat Output

This is a programmable, periodic pulse with a TTL driver. It is present regardless of whether the board is synchronized or freewheeling. The power on default setting for the heartbeat output is **off**.

1.15 Match Output

The Match Output goes high at a preset time and low at another preset time, much like an alarm clock. It is a TTL output.

1.16 In-Sync Output

This is the same signal that lights the green SYNC light on the front panel and drives the Flag - Sync bit in the Status Register. It is an open-collector output, suitable for driving an LED or a small relay. It can also be used to drive TTL logic by connecting an external 4.7K pull-up resistor to +5V. Use of a Schmitt Trigger (e.g. - 74HCT14) input is recommended, as the rise time will be relatively slow. Rise time is determined by the external pull-up resistor and the distributed cable capacitance.

The In-Sync output conducts current to ground when the board is in-sync with GPS or the timecode input. It also pulses low briefly during power-on reset, or when a Forced Reset or Lamp Test command is issued. This provides a means of testing the external relay or LED.

1.17 Indicator Lights

The front panel has two indicator lights.

1.17.1 ACQ Indicator Light

The yellow ACQ indicator is lighted when the board is in the process of acquiring either the GPS satellite signals or the incoming timecode. The ACQ indicator is not lighted if the timecode input is not present, nor if the serial communication to the GPS receiver has errors, or if the board is in-sync.

The ACQ indicator is also lighted momentarily during power-on reset, or when a Forced Reset or Lamp Test command is issued, or when any command is sent to the board when the Blink Yellow Mode is enabled.

1.17.2 SYNC Indicator Light

The green SYNC indicator lights when the board has established synchronization with the GPS satellite signal, or input timecode.

The SYNC indicator is also lighted momentarily during power-on reset, or when a Forced Reset or Lamp Test command is issued.

2 Specifications

NOTE: Specifications are applicable to both TPRO-PMC and TSAT-PMC unless otherwise stated.

2.1 General

Size (board)	74 mm,149 mm, 1.6mm (H,D,T) (2.91 inch, 5.87 inch, 0.063 inch) (H,D,T)
Size (front panel)	CMC bezel x 4HP 74 mm, 12.70 mm (H,W) (2.91 inch, 0.50 inch) (H,W)
Circuit Board Material	UL 94V-0 FR-4
Power (TSAT-PMC)	+5V ± 5%: 425 mA max +12V ± 5%: 425 mA max -12V ± 5%: 50 mA max
Power (TPRO-PMC)	+5V ± 5%: 425 mA max +12V ± 5%: 225 mA max -12V ± 5%: 50 mA max
Operating Temperature	TSAT-PMC: 0 to 70 C (32 to 158 F) TPRO-PMC: 0 to 70 C (32 to 158 F)
Storage Temperature	-40C to +85C (-40F to +185F)
Humidity	0 to 95%, non-condensing
TIMING Connector	Commercial Micro – D Socket, 15 pins
GPS ANTENNA Connector	Commercial Micro – D Plug, 15 pins

2.2 PCI Mezzanine® (PMC) Interface

PCI Mezzanine® Interface	Standard 32-bit (PMC1J1, PMC1J2)
PCI Mezzanine® Spec	IEEE Std 1386.1 - 2001 Compliant
Memory Map	64 consecutive 32-bit words (256 bytes)
I/O Map	(none)
Chipset Vendor ID (PLX Technology, Inc.)	0x10b5
Chipset Device ID (PLX 9050 Chip)	0x9050
Subsystem Vendor ID (Spectracom)	0x1347
Subsystem Device ID (TPRO-PMC)	0x 7200
Subsystem Device ID (TSAT-PMC)	0x 7300

2.3 On-board Clock

Synchronization to GPS (TSAT-PMC)	±1 uS max
Synchronization to Timecode Input (TPRO-PMC)	±10 uS max (IRIG-A) ±15 uS max (IRIG-B, NASA36)
Timebase (freewheeling)	TSAT-PMC: ±1 PPM in one minute TPRO-PMC: ±10 PPM in one minute
Range	366:23:59:59.999999
Resolution	1 uS

2.4 External GPS Receiver/Antenna (TSAT-PMC Only)

Number of Satellites Tracked	12 max
Acquisition Time (Warm Start)	45 seconds (typical)
Acquisition Time (Cold Start)	2 minutes (typ), 15 minutes (max)
Frequency	1575.42 MHz (Receive Only, L1 Band, C/A Code, SPS)
Sync to UTC	±130 nS (1 sigma, stationary location)
Altitude	-400 m to +8,000 m (-1,312 ft to +25,000 ft)
Position Accuracy	40 meters (135 ft) 2dRMS
Datum	WGS-84
Operating Temperature	-30C to +75C (-20F to +165F)
Storage Temperature	-55C to +90C (-65F to +195F)
Humidity	MIL STD 810E, Method 507.3, Procedure I, II, III (95%)
Weatherproof	MIL STD 810E, Method 512.3
Salt Fog	MIL STD 810E, Method 509.3 (48 hours)
Ultraviolet Protection	ASTM G53-88
Transient Protection	600 Watts, 1 mS (data and power lines)
ESD	IEC 1000-4-2 Level 4 (-8 KV to +8 KV)
EMI	FCC Part 15 Class B, European CE
Size	115 mm, 90 mm (4.5 inch, 3.6 inch) (Dia., H)
Mass	475 g (16.8 oz.)
Mounting	1-14 UNS threads x 1 inch deep
Mating Connector	Deutsch MMP26C-2212S1 Plug Housing with Deutsch 6862-201-22278 Contact Sockets

2.5 Supplied GPS Antenna Cable (TSAT-PMC Only)

Length	30.5 m ± 0.3 m (100 ft ± 1 ft)
Cable Size	9 mm (0.4 inch) O.D.
Antenna Connector Size	20 mm (0.8 inch) O.D.
Board Connector Size	34 mm X 16 mm (1.4 inch x 0.6 inch)
Outer Jacket	Black PVC with U/V Stabilizer/Inhibitor
Internal Wires	5 Twisted Pairs, 22 AWG, stranded, insulated wire
EMI Shield	Foil (100% Coverage) and drain wire

2.6 Optional Extension Cable for TSAT-PMC (TRIM-CAB-PMC-100)

Length	30.3 m ± 0.3 m (99.5 ft ± 1 ft)
Cable Size	9 mm (0.4 inch) O.D.
Connector Size (both ends)	34 mm X 16 mm (1.4 inch x 0.6 inch)

2.7 Timecode Input (TPRO-PMC)

Connector	Comm Micro –D 25 *TIMING*, Pins 12 and 13
Format (detected automatically)	IRIG-B(122) or IRIG-A(132)
Amplitude (mark) IRIG-A Amplitude (mark) IRIG-B	1.2 Vp-p (min), 8.0 Vp-p (max) 1.2 Vp-p (min), 8.0 Vp-p (max)
Modulation Ratio	2:1 min, 3:1 typical, 4:1 max
Time Base Error	±25 ppm max
Input Impedance	10K ohm
Common-Mode Voltage (relative to signal ground)	±100 V max
Acquisition Time	15 seconds max

2.8 Timecode Output

Connector	Comm Micro –D 25 *TIMING*, pin 10
Format	IRIG-B(122)(CF and SBS fields not used)
Amplitude (mark)	3.0 Vp-p min, 4.0 Vp-p typical, 6.5 Vp-p max; into 50 ohms
Modulation Ratio	3:1 (typical)
Timebase Error	same as specified for the on-board clock

2.9 Time Tag Input

Connector	Comm Micro –D 25 *TIMING*, pin 16
Tagged Edge	Rising
Input Voltage (high)	+2.2 V min, +5.1 V max
Input Voltage (low)	-0.1 V min, +0.4 V max
Input Current (high)	100 uA max
Input Current (low)	-600 uA max
Input Termination (on-board)	10.7K ohms to +5 Volts
Rise/Fall Time	150 nS max
Pulse Width (time high)	1 uS min, 999.999 mS max
Time Between Each Rising Edge	500 uS min
Repetition Rate	2000 events/second max
Time Tag Accuracy	± 1 uS

2.10 1PPS Output

Connector	Comm Micro -D 25 *TIMING*, pins 1 and 2
Output Type	Differential RS-422
Recommended Termination	120-ohms, ½ watt, line-to-line
On-Time Edge	Rising
Timebase Error	same as on-board clock
Differential Output Voltage	3.0 Vp-p typical into 120 ohms
Output Skew (pin 13 to pin 12)	5 nS typical
Pulse Width	4 uS typical

2.11 Oscillator Output

Connector	Comm Micro -D 25 *TIMING*, pins 6 and 7
Output	Off, 1 kHz, 1 MHz, 5 MHz, or 10 MHz (programmable)
Power-on Default Frequency	Off
Output Type	Differential RS-422
Wave Shape	Squarewave, 40%/60% duty cycle
Recommended Termination	120-ohms, ½ Watt, line-to-line
Differential Output (into 120 ohms)	2.5 Vp-p (1 kHz or 1 MHz) 2.0 Vp-p (5 MHz) 1.7 Vp-p (10 MHz)
Output Skew (pin 8 to pin 15)	5 nS typical
Cable Length* (1 kHz or 1 MHz)	76 m (250 ft) max
Cable Length* (5 MHz)	23 m (75 ft) max
Cable Length* (10 MHz)	3 m (10 ft) max

** Recommended cable is 22 AWG twisted, shielded pair. Connect shield to connector shell.*

2.12 Heartbeat Output

Connector	Comm Micro -D 25 *TIMING*, pin 5
Wave Shape	Pulse
Pulse Polarity	Programmable
Pulse Width	100 nS, 333 nS, 1 uS, or 1 mS (Programmable)
Output Voltage (high)	2.4 V min at 2.5 mA
Output Voltage (low)	0.4 V max at -2.5 mA
Output Current (high or low)	2.5 mA max
Range	200 nS to 65.5 Seconds
Power-on Default	Disabled

2.13 Match Output

Connector	Comm Micro -D 25 TIMING, pin 3
Output Voltage (high)	3.8 V at 4 mA
Output Voltage (low)	0.3 V at -4 mA
Output Current (high or low)	±6 mA max
Setability	1 uS
Timebase Error	same as on-board clock

2.14 In-Sync Output

	Comm Micro -D 25 TIMING, pin 17
Output Type	Open Collector
External Pull-up Voltage	+27 VDC max
Output Voltage (low)	+0.5 V max at -20 mA
Output Current (low)	-20 mA max

CAUTION:

An external diode is required when driving inductive loads (e.g. - relays). The diode should be physically located as close to the load as possible, connected across the load so that it is reverse-biased when this output is low. The user is responsible for choosing the proper diode, capable of suppressing the induced energy from the collapsing magnetic field.

3 Register Level Description

3.1 Numbering Conventions

Throughout this manual, hexadecimal number values are denoted with the "0x" prefix. For example, "0x1234" represents the hexadecimal value "1234", which is 4660 in decimal notation, and "0001 0010 0011 0100" in binary notation.

Also, "\0" denotes the single ASCII "null" character, which has a value of zero (0x00). It indicates the end of an ASCII string.

3.2 Base Address

All accesses to the board consist of reading or writing 32-bit word values. The base address is assigned at power-on by the BIOS software. The absolute memory address is computed as the Base Address plus a constant Offset. Addresses count bytes (8 bits), but data is transferred as words (32 bits). Thus, the offset for each register is a number evenly divisible by four.

NOTE: Some of the registers use less than 32-bits. For clarity, only those bits actually used are described in this manual. All unused bits must be ignored to maintain compatibility with future revisions.

3.3 ASCII Strings

Some of the commands and responses consist of ASCII strings. Four ASCII bytes are grouped together in a single 32-bit word. The first character in the string is in the lowermost part of the word (bits 07:00), the next character byte is in bits 15:08, the next is in bits 23:16, and the fourth character in the string is in bits 31:24. For responses, which use more than four characters, the fifth character is in bits 07:00 of the word located at the next (higher) address, etc.

The “null” character denotes the end of an ASCII string. This is a single 8-bit number, value 0x00, and is written as "\0" in this manual. For example, the string "TEST12.3456\0" stored in the Response Register (tbreg_response[0] through tbreg_response[3]) would appear in memory as:

Offset	*Contents*	*Description*			
0x30	0x54534554	'T'	'S'	'E'	'T'
0x34	0x332e3231	'3'	'.'	'2'	'1'
0x38	0x00363534	'\0'	'6'	'5'	'4'
0x3c	0x????1234	Echo of command 0x1234			

(? denotes an undefined value)

Not all commands and responses are ASCII strings. Some use straight binary format, and others use Binary Coded Decimal (BCD) format.

3.4 Register Map

The registers are mapped into 64 words (256 bytes) of consecutive memory space as shown below. The absolute memory address is computed as Base+Offset. "tbreg_" means "timing board register."

For some registers, the content of the data written is irrelevant; the act of writing (any value) to the register triggers an event.

Offset	*Name (read)*	*Name (write)*
0x00	tbreg_status	tbreg_irq_enable
0x04	tbreg_clk_upper	tbreg_clrflag_m
0x08	tbreg_clk_lower	tbreg_clrflag_hb
0x0c	tbreg_clk_date	tbreg_clrflag_cmov
0x10	tbreg_ttag_status	tbreg_sim_ttag
0x14	tbreg_ttag_upper	tbreg_clrflag_sc
0x18	tbreg_ttag_lower	
0x1c	tbreg_ttag_date	
0x20		tbreg_cmd[0]
0x24		tbreg_cmd[1]
0x28		tbreg_cmd[2]
0x2c		tbreg_cmd[3]
0x30	tbreg_response[0]	
0x34	tbreg_response[1]	
0x38	tbreg_response[2]	
0x3c	tbreg_response[3]	
0x40		tbreg_reset

0x44 through 0xfc are reserved for future use.

3.4.1 Forced Reset (tbreg_reset)

Writing (any value) causes the board's embedded microprocessor to be reset. The board's bus interface logic is not reset. The user must wait for eight seconds after issuing this command before accessing the board.

3.4.2 Command Register (tbreg_cmd[3:0])

Commands are sent to the board by writing parameters (if any) to tbreg_cmd[2:0], then writing the command code to tbreg_cmd[3]. Commands are described in detail in Section 4.

3.4.3 Response Register (tbreg_response[3:0])

Responses to commands are placed in the response register. Responses are described in detail in Section 5.

3.4.4 Interrupt Enable Register (tbreg_irq_en)

The user can specify which of several possible conditions will generate an interrupt. The individual bits correspond to the IRQ Enable bits in the Status Register.

3.4.5 Clear Flag - Match Register (tbreg_clrflag_m)

Writing (any value) clears Flag - Match.

3.4.6 Clear Flag - Heartbeat Register (tbreg_clrflag_hb)

Writing (any value) clears Flag - Heartbeat.

3.4.7 Clear Flag - Command Overflow (tbreg_clrflag_cmov)

Writing (any value) clears Flag - Command Overflow.

3.4.8 Clear Flag - Sync Change (tbreg_clrflag_sc)

Writing (any value) clears Flag - Sync Change.

3.4.9 Status Register (tbreg_status)

The Status Register is defined as shown below. Reading the Status Register also loads the instantaneous Clock Time and Clock Date Registers.

Bit	*Name*	*Definition (1=asserted)*
31:30		(reserved for future use)
29	tbstat_f_cmov	Flag - Command Overflow
28	tbstat_tp_int	Testpoint - Interrupt
27:24	tbstat_ttec[3:0]	Time Tag Event Counter
23:21		(reserved for future use)
20	tbstat_tp_gps	Testpoint - GPS Antenna
19		(reserved for future use)
18:16	tbstat_ssi[2:0]	Synchronization Source Indicator
15		(reserved for future use)
14	tbstat_ttenable	Enable/disable Time Tag input
13	tbstat_irq_sc	IRQ Enable - Sync Change
12	tbstat_irq_cc	IRQ Enable -Command Complete
11		(reserved for future use)
10	tbstat_irq_tt	IRQ Enable - Time Tag
09	tbstat_irq_hb	IRQ Enable - Heartbeat
08	tbstat_irq_m	IRQ Enable - Match
07	tbstat_f_sc	Flag - Sync Change
06	tbstat_f_cc	Flag - Command Complete
05		(reserved for future use)
04	tbstat_f_tt	Flag - Time Tag
03	tbstat_f_hb	Flag - Heartbeat
02	tbstat_f_m	Flag - Match
01	tbstat_f_sync	Flag - Sync
00	tbstat_f_acq	Flag - Acquire

3.4.9.1 Flag - Acquire

This status bit is asserted when the board detects that a timecode is present (before synchronization is established), or when the GPS receiver is connected, but not tracking satellites. It is not asserted if no timecode is connected to the input.

This bit corresponds to the yellow ACQ panel indicator, except this bit is not asserted during the lamp test or in response to a command while in Blink Yellow Mode.

3.4.9.2 Flag - Sync

This is the only bit to examine to determine if the board has established synchronization. It is asserted when the board is properly synchronized to the incoming timecode, or to the GPS satellites. It also indicates that the computed longitude, latitude, and altitude are valid (TSAT-PMC).

This bit corresponds to the green SYNC panel indicator, except this bit is not asserted during the lamp test.

3.4.9.3 Flag - Command Overflow

This bit is intended to be a tool for debugging user-written software. It is asserted if the user's software sends a command (writes to tbreg_cmd[3]) when the board is not ready to accept a new command. It is de-asserted by writing (any value) to tbreg_clrflag_cmov.

3.4.9.4 Flag - Match

Asserted when the Match Start time occurs. Reset this bit by writing (any value) to the tbreg_clrflag_m register. The Match Stop time does not affect it. This bit might be set at power-on reset; the user must clear this bit before setting the Match Start time.

3.4.9.5 Flag - Heartbeat

Each Heartbeat pulse sets this flag; the user clears it by writing (any value) to tbreg_clrflag_hb. The user's software must be fast enough to clear each Heartbeat before the next one occurs. This bit might be set at power-on reset; the user must clear this bit before using it.

The next Heartbeat output pulse will happen regardless of whether the user has cleared this flag. The user's software does not need to clear the Heartbeat Flag if the user's software does not interrogate this flag.

3.4.9.6 Flag - Time Tag

This is asserted when a Time Tag event occurs. The user acknowledges the Time Tag event, and de-asserts this bit, by reading the tbreg_ttag_date. This bit might be set at power-on reset; the user must clear this bit before using it.

3.4.9.7 Flag - Command Complete

This indicates that the board is ready to accept a new command in the tbreg_cmd[3:0] register. Writing to tbreg_cmd[0] clears this bit. The board will assert it after processing the command. The user must always check that this bit is asserted before sending a command.

3.4.9.8 Flag - Sync Change

This bit is asserted when Flag - Sync changes state, either from not in sync to in sync, or vice versa. Writing (any value) resets it to tbreg_clrflag_sc.

3.4.9.9 Interrupt Enables

These six bits are asserted or de-asserted by writing to the corresponding bits in the Interrupt Enable Register. The user can read-back these bits by reading the Status Register. Writing "1" enables the interrupt. The power-on default is "0".

The interrupt will be asserted as long as the Interrupt Enable and Flag bits are both "1". Be sure that the corresponding flag bit is not asserted before setting the Interrupt Enable bit, otherwise, an unexpected interrupt will occur. The user's interrupt handler software acknowledges the interrupt by clearing the corresponding flag bit.

3.4.9.10 IRQ Enable - Match

Enables an interrupt when Flag - Match is asserted.

3.4.9.11 IRQ Enable - Heartbeat

Enables an interrupt when Flag - Heartbeat is asserted.

3.4.9.12 IRQ Enable - Time Tag

Enables an interrupt when Flag - Time Tag is asserted.

3.4.9.13 IRQ Enable - Command Complete

Enables an interrupt when Flag - Command Complete is asserted.

Use this interrupt carefully. The only way to clear Flag - Command Complete is to send another command. This interrupt might be useful if a series of commands are to be sent, but most applications will not use this feature.

3.4.9.14 IRQ Enable - Sync Change

Enables an interrupt when Flag - Sync Change is asserted. This is useful for determining that synchronization has been established or lost.

3.4.9.15 Enable/Disable Time Tag Input

This bit enables (1) or disables (0) the Time Tag Input on the TIMING connector. Write "1" or "0" to the corresponding bit in the Interrupt Enable Register. The user can read-back this bit by reading the Status Register. The power-on default is "0" (disabled).

3.4.9.16 Synchronization Source Indicator

These three bits indicate which input time source is being used. This is intended for diagnostic purposes only.

tbstat_ssi[2:0]	Input Time Source
000	Searching for timecode input (TPRO-PMC) Acquiring GPS satellites (TSAT-PMC)
001	Timecode Input (IRIG-A autodetected)
010	Timecode Input (IRIG-B autodetected)
011	Timecode Input (NASA36 autodetected)
100	GPS Satellites
Others	Reserved for future use

3.4.9.17 Time Tag Event Counter

This is intended for diagnostic purposes only. It counts the number of time tag events that have occurred since the time tag registers were read. If it reaches maximum count (0xf) it will remain at maximum count.

The board only latches one time tag event. If another event occurs before the user reads the time tag registers, the second event will be lost (not latched). This counter can be used to determine if time tag events are being lost. Read this counter immediately prior to reading the time tag registers. If the count is zero, no events have occurred. If it is one, the time tag registers contain the latest event time, and no events have been lost. If it is greater than one, some time tag events have been lost.

The user's software must be able to read the time tag register faster than the event repetition rate. External hardware can be used to divide the time tag signal, so only every fifth event is tagged (for example). Such hardware is the user's responsibility.

3.4.9.18 Testpoint - Interrupt

This status bit is asserted when the board is asserting an interrupt. This is for diagnostic purposes only. The user should only examine the Flag bits, in conjunction with the IRQ Enable bits, to determine which interrupt to service.

3.4.9.19 Testpoint - GPS Antenna

The board receives various messages from the GPS receiver/antenna. This bit is asserted when the board determines that the received messages are in the proper format. This does not indicate that it is tracking satellites; it only means that the communication between the board and the receiver/antenna is functioning properly.

If this bit is not asserted, the most likely problem is that the antenna cable is disconnected.

This bit will not be asserted during the first few seconds after a power-on reset or Forced Reset command.

The TPRO-PMC will always de-assert this bit. For this reason, do not use this bit to disqualify the board's data. Instead, use this bit only as a troubleshooting tool.

3.4.10 Clock Time Registers

(tbreg_clk_upper, tbreg_clk_lower, and tbreg_clk_date)

To read the Clock Time, first read the Status Register as described above, then read the two Clock Time registers and the Clock Date register. These registers consist of groups of four bits, each of which represents a digit in the time (i.e. - it is in Binary Coded Decimal (BCD) format).

Bits	tbreg_clk_upper	tbreg_clk_lower
31:28	(reserved)	10s of seconds
27:24	100s of days	1s of seconds
23:20	10s of days	100s of mS
19:16	1s of days	10s of mS
15:12	10s of hours	1s of mS
11:08	1s of hours	100s of µS
07:04	10s of minutes	10s of µS
03:00	1s of minutes	1s of µS

For example, the time day 123, hour 09, minute 41, second 36.456789 would be represented as:

tbreg_clk_upper = 0x?1230941
tbreg_clk_lower = 0x36456789

(? denotes an undefined value)

4 Commands and Responses

4.1 Introduction

To send a command:

1.) Read the Status Register, do not proceed until *Flag - Command Complete* = 1.

2.) Write the command to tbreg_cmd[3:0]. *Important*: Write to tbreg_cmd[3] last.

3.) If a response is expected, read the Status Register until *Flag - Command Complete* = 1, then read the response from tbreg_response[3:0].

Bits 15:00 of tbreg_cmd[3] specify the command operand. To maintain compatibility with future products, write zeroes to fields listed as "(unused)".

Writing to tbreg_cmd[3] causes the *Flag - Command Complete* status bit to be de-asserted, and signals the board to begin processing the command. This status bit is asserted *after* the board finishes processing the command. Only one command can be processed at a time.

4.2 Set Time (0 x 0010)

When not synced to GPS or incoming timecode, the time can be set by the host computer. The time will then continue to increment from the set value (freewheel). However, if the GPS receiver begins tracking satellites, or if a timecode input is applied, time will jump to the GPS or timecode time (unless synchronization has been disabled by the *Disable Sync* command).

Set Time values are specified from days through seconds. The milliseconds and microseconds are reset to zero when the command is processed. The time is formatted as Binary Coded Decimal (BCD).

Bits	*tbreg_cmd[0]*
31:28	(unused)
27:24	100s of days
23:20	10s of days
19:16	1s of days
15:12	10s of hours
11:08	1s of hours
07:04	10s of minutes
03:00	1s of minutes

Bits	*tbreg_cmd[1]*
31:28	10s of seconds
27:24	1s of seconds
23:00	(unused)

Bits	*tbreg_cmd[2]*	*Bits*	*tbreg_cmd[3]*
31:16	(unused)	31:16	(unused)
15:12	1000s of Year	15:00	0x0010
11:08	100s of Year		
07:04	10s of Year		
03:00	1s of Year		

For example, to set the board to year 2001, day 345, hour 12, minute 56, second 29, write the following values:

tbreg_cmd[0] = 0x03451256
tbreg_cmd[1] = 0x29000000
tbreg_cmd[2] = 0x00002001
tbreg_cmd[3] = 0x00000010

The board will compute the Gregorian date (December 11) from the Julian day (345) and the year. Leap years are taken into account.

The year is used to determine whether the board should count to day 365 (non-leap year) or 366 (leap year) before rolling back to 001. The year *is not* transmitted in the timecode output, so each board in a system must be commanded separately. The year *is not* used in the Match Time comparison. The power-on default is the special year 0001, a non-leap year. TSAT-PMC boards obtain the year from the GPS satellites, or it can be set manually, as described above. The year is incremented at the end of day 365 or 366.

A leap year is any year that is evenly divisible by four, except century years. A century year (2000, 2100, etc.) is a leap year only if it is evenly divisible by 400 (e.g. - 2000, 2400, etc.).

The response in tbreg_response[3] is 0x????0010.

The user's software must ensure that only valid values are sent to the board. Also, the year must be set before the day. Otherwise, invalid Gregorian dates may result.

Field	*Range*
Day	000-366
Hour	00-23
Minute	00-59
Second	00-59
Year	1990-2999

CAUTION:

The board does not check the range on these parameters. Sending out-of-range values will result in erroneous operation. This applies to all command.

4.3 Set Year (0 x 0015)

Timecodes (IRIG-A, IRIG-B and NASA36) do not convey the year. Use this command to set the year. This is the same as setting the year using the 0x0010 command, except that this command does not change the Julian day or time. The year can be specified regardless of whether the board is in sync or not, and the year is retained if the board loses/acquires sync.

The valid range is 1990-2999. Values outside this range will result in the year being set to 0001.

Bits	*tbreg_cmd[0]*
31:00	(unused)

Bits	*tbreg_cmd[1]*
31:00	(unused)

Bits	*tbreg_cmd[2]*
31:16	(unused)
15:12	1000s of Year
11:08	100s of Year
07:04	10s of Year
03:00	1s of Year

Bits	*tbreg_cmd[3]*
31:16	(unused)
15:00	0x0015

For example, to set the year to 2003, write the following commands:

tbreg_cmd[2] = 0x00002003
tbreg_cmd[3] = 0x00000015

The response indicates that the year has been set, or indicates year 0001 if an invalid year was commanded. The response is:

Bits	*tbreg_response[0]*
31:00	(unused)

Bits	*tbreg_response[1]*
31:00	(unused)

Bits	*tbreg_response[2]*
31:16	(unused)
15:12	1000s of Year
11:08	100s of Year
07:04	10s of Year
03:00	1s of Year

Bits	*tbreg_response[3]*
31:16	(unused)
15:00	0x0015

4.4 Set Match Start Time (0 x 0020)

Set the Match Start time by writing the following values:

Bits	*tbreg_cmd[0]*	*Bits*	*tbreg_cmd[1]*
31:28	(unused)	31:28	10s of seconds
27:24	100s of days	27:24	1s of seconds
23:20	10s of days	23:20	0.1s of seconds
19:16	1s of days	19:16	0.01s of seconds
15:12	10s of hours	15:12	0.001s of seconds
11:08	1s of hours	11:08	0.0001s of seconds
07:04	10s of minutes	07:04	0.00001s of seconds
03:00	1s of minutes	03:00	0.000001s of seconds

Bits	*tbreg_cmd[2]*	*Bits*	*tbreg_cmd[3]*
31:00	(unused)	31:16	(unused)
		15:00	0x0020

For example, to specify a Match Start time of day 345, hour 12, minute 56, second 29.123456, write the following values:

tbreg_cmd[0] = 0x03451256
tbreg_cmd[1] = 0x29123456
tbreg_cmd[3] = 0x00000020

The MATCH output and *Flag - Match* will be asserted when the clock time equals the Match Start time. The year is not used in the comparison. This command must be sent at least 50 mS prior to this.

The response in tbreg_response[3] is 0x00010020 if all fields are valid, or 0x00000020 if any field was out of range, specifically:

Field	*Range*
Day	000-366
Hour	00-23
Minute	00-59
Second	00-59

4.5 Set Match Stop Time (0 x 0030)

Set the Match Stop Time as described above, except write tbreg_cmd[3] = 0x00000030. The response in tbreg_response[3] is 0x00010030 if all fields are valid, or 0x00000030 if any field was out of range.

4.6 Set Heartbeat Divider (0 x 0040)

The Heartbeat is the output of a programmable divider. This command selects the clock frequency and the counter preset number.

The counter counts from the counter preset number up to maximum count (0xffff). When maximum count is reached, one Heartbeat pulse is output, and the counter re-loads the counter preset number. Compute the counter preset number N as follows:

N = 65536 - (F * t)

F is the frequency chosen, t is the Heartbeat interval in seconds.

The permissible range of values for N depends on the clock select. For clock selects 0x0, 0x2, and 0x3, the permissible range for N is 0x0000 through 0xfffe, inclusive. However, for clock select 0x1, the permissible range is 0x0003 through 0xfffc, with the further restriction that N must be evenly divisible by 3.

Set the Heartbeat period as follows. The counter will be forced to maximum count each time synchronization is established. This causes the Heartbeat output to be in sync with the absolute time.

Bits	*tbreg_cmd[0]*	*Bits*	*tbreg_cmd[1]*
31:16	(unused)	31:04	(unused)
15:00	N	03	Invert(1)/Normal (0)
		02	Enable(1)/Disable (0)
		01:00	Clock Select

Bits	*tbreg_cmd[2]*	*Bits*	*tbreg_cmd[3]*
31:00	(unused)	31:16	(unused)
		15:00	0x0040

The Clock Select field selects F, as follows:

Clock Sel	*F*	*Pulse Width*	*Programmable Range Minimum*	*Maximum*
0x0	$1 * 10^7$	100 nS	200 nS	6.55 mS
0x1	$3 * 10^6$	333 nS	666 nS	21.84 mS
0x2	$1 * 10^6$	1 µuS	2 µS	65.5 mS
0x3	$1 * 10^3$	1 mS	2 mS	65.5 seconds

Step size is the same as the Pulse Width.

4.6.1 Examples for Setting the Heartbeat

If the desired Heartbeat interval is 750 uS between pulses, choose ($1 * 10^6$) for the Clock Select, and compute N = 0xfd12:

$N = 65536 - (1 * 10^6)*(750 * 10^{-6})$
N = 64786 (base 10) convert to hex: 64786 = 0xfd12

Other examples:

Desired Pulse Rate	*Chosen Clock Select*	*N*
1.25 MPPS	0x0 ($1 * 10^7$)	0xfff8
120 PPS	0x1 ($3 * 10^6$)	0x9e58
100 PPS	0x2 ($1 * 10^6$)	0xd8f0
0.1 PPS	0x3 ($1 * 10^3$)	0xd8f0

Notice that, although 120 PPS and 100 PPS are in the range of clock selects 0x2 and 0x3, the clock select must be chosen to divide evenly.

4.7 Select Oscillator Output Frequency (0 x 0 n 45)

Select the frequency for the Oscillator Output. Write one of the following commands to tbreg_cmd[3] to specify the frequency. The power-on default is OFF. Read tbreg_response[3] after sending the command to verify that it has been accepted.

Frequency	*Command*	*Response*
Off	0x00000045	0x????0045
1 kHz	0x00000145	0x????0145
1 MHz	0x00000245	0x????0245
5 MHz	0x00000345	0x????0345
10 MHz	0x00000445	0x????0445

If invalid data is commanded in bits 15:08, the response will be 0x????ff45, and the output will be OFF.

4.8 Set Offset Time (0 x 0060)

This command is used to introduce deliberate offsets into the time. Most applications use the power-on default (zero delay). Setting a deliberate offset is useful for providing a pre-trigger. For example, the board's 1PPS output could be used to trigger an instrument at a known time *before* an event.

Offset times range from -999 to +999 µS in 1 µS steps. Negative numbers move the board's time earlier relative to actual time. The offset is coded in BCD format. There is no response.

The board implements the offset by varying the oscillator frequency until the board's time is changed by the commanded offset. Thus, it may take up to 5 minutes for an offset to take effect.

Bits	tbreg_cmd[0]	Bits	tbreg_cmd[1]
31:16	(unused)	31:00	(unused)
15:0	N		

Bits	tbreg_cmd[2]	Bits	tbreg_cmd[3]
31:00	(unused)	31:16	(unused)
		15:00	0x0060

Compute N as follows:

For negative offsets:

N = offset (range 0x0000 through 0x0999)

For positive offsets:

N = 0x1000 + offset (range 0x1000 through 0x1999)

NOTE: Be careful when writing software to increment or decrement this value. Only BCD values are acceptable. For example, 0x0019 and 0x0020 are valid, but 0x001A is not. Invalid values will be ignored.

4.9 Read Number of Satellites Tracked & Altitude (0 x 0070) (TSAT-PMC Only)

Write command 0x00000070 to tbreg_cmd[3] to determine how many GPS satellites are being tracked, and the computed altitude (elevation). Altitude units are "meters above mean sea level." An ASCII string is returned. This contains the number (quantity) of satellites being tracked, and the altitude.

Bits	tbreg_response[0]	tbreg_response[1]	
31:24	fourth character	31:24	eight character
23:16	third character	23:16	seventh character
15:08	second character	15:08	sixth character
07:00	first character	07:00	fifth character

Bits	tbreg_response[2]	tbreg_response[3]	
31:24	twelfth character	31:16	(unused)
23:16	eleventh character	15:00	0x0070
15:08	tenth character		
07:00	ninth character		

The response string is formatted as "AAAA.A,M,SS\0" where AAAA.A is the altitude and SS is the number of satellites tracked. The fields are delimited by commas, might (or might not) include leading zeroes, and may vary in length. Altitudes below mean sea level begin with "-".

The "-" can appear in any of the “A” fields. Therefore you could have the following combinations: (-999.9), (0-99.9), (00-9.9), (000-.9), but altitudes above mean sea level do *not* begin with "+". Some antennas may not support below sea level conditions.

For example, "235.0,07\0" means it is tracking 7 satellites, and the computed altitude is 235.0 meters above mean sea level. The resolution of the altitude field may exceed the accuracy of the altitude computation. Empty fields may be present when it is not tracking satellites (e.g. ",\0").

4.10 Read Longitude (0 x 0071) (TSAT-PMC Only)

Write command 0x00000071 to tbreg_cmd[3] to read the computed longitude. Units are degrees, minutes, and fractional minutes, *not* degrees, minutes, and seconds. An ASCII string is returned.

Bits	*tbreg_response[0]*	*tbreg_response[1]*	
31:24	fourth character	31:24	eight character
23:16	third character	23:16	seventh character
15:08	second character	15:08	sixth character
07:00	first character	07:00	fifth character

Bits	*tbreg_response[2]*	*tbreg_response[3]*	
31:24	twelfth character	31:16	(unused)
23:16	eleventh character	15:00	0x0071
15:08	tenth character		
07:00	ninth character		

The response format is "DDDMM.FFFFZ\0" where DDD is degrees, MM is minutes, FFFF is fractional minutes, and Z is either 'E' or 'W' (East or West). For example, "07123.4561W\0" represents 71 degrees, 23.4561 minutes, West. Empty fields may be present when it is not tracking satellites. While tracking satellites, leading zeroes will be present in the DDD, MM, and FFFF fields, if necessary, to maintain constant field size.

4.11 Read Latitude (0 x 0072) (TSAT-PMC Only)

Write command 0x00000072 to tbreg_cmd[3] to read the computed latitude. Units are degrees, minutes, and fractional minutes, *not* degrees, minutes, and seconds. An ASCII string is returned.

Bits	*tbreg_response[0]*	*tbreg_response[1]*
31:24	fourth character	eight character
23:16	third character	seventh character
15:08	second character	sixth character
07:00	first character	fifth character

Bits	*tbreg_response[2]*	*tbreg_response[3]*
31:24	twelfth character	(unused)
23:16	eleventh character	0x0072
15:08	tenth character	
07:00	ninth character	

The response format is "DDMM.FFFFZ\0" where DD is degrees, MM is minutes, FFFF is fractional minutes, and Z is 'N' or 'S' (North or South). Empty fields may be returned when it is not tracking satellites (e. g. "\0"). While tracking satellites, leading zeroes will be present in the DD, MM, and FFFF fields, if necessary, to maintain constant field size.

4.12 Enable/Disable Synchronization Flat (0 x 00c0 and 0 x 00c1)

To disable synchronization to GPS, timecode input, or 1PPS input, write command 0x000000c0 to tbreg_cmd[3]. To re-enable synchronization, send command 0x000000c1. The power-on default is to enable synchronization. There is no response.

4.13 Read Synchronization Enable Flag (0 x 00c2)

To read the synchronization enable status, send command 0x000000c2 to tbreg_cmd[3]. The response in tbreg_response[3] will be 0x000001c2 if synchronization is enabled, or 0x000000c2 if disabled.

4.14 Factory Test Messages (0 x 00eb, 0 x 01eb, ...)

The Factory Test Messages provide a means of diagnosing problems. There are 16 different possible messages, each of which is 128 bits (4 words) long. Spectracom recommends that the user include the ability to read these messages. Specifically, the user's software should include a function (subroutine) to read and display them (or log them to the disk). Normally, this function (subroutine) is not called.

The exact meaning of these messages is proprietary, and is not disclosed in this manual. Each response consists of data in tbreg_response[3:0]. As with other commands, the command is echoed in tbreg_response[3], bits 15:00.

To read one of the messages, send the appropriate command to tbreg_cmd[3], then read tbreg_response[0], tbreg_response[1], tbreg_response[2], and tbreg_response[3]. The commands are as follows:

Command	*Response*
0x000000eb	Factory Test Message 00
0x000001eb	Factory Test Message 01
0x000002eb	Factory Test Message 02
...	...
0x00000feb	Factory Test Message 15

NOTE: Spectracom may ask for the firmware and FPGA versions during troubleshooting. The function (subroutine) for reading the Factory Test Messages should also read these, as described in the next section.

4.15 Read Version (0 x 00ec)

This allows the user to read the version numbers of the FPGA (field-programmable gate array) and the embedded firmware. It is *not* possible to determine what options are present, or which version is more recent, from this number. This is for diagnostic purposes only. We suggest that the user's software should include a means of reading and displaying these numbers.

Send command 0x000000ec to tbreg_cmd[3]. The FPGA version is reported in bits 23:00 of tbreg_response[0]. The embedded firmware version is reported in bits 23:00 of tbreg_response[2]. These are in hexadecimal format.

For example, if the FPGA version is 033000 and the firmware version is 032900, the response will be:

tbreg_response[0] = 0x??033000
tbreg_response[1] = 0x????????
tbreg_response[2] = 0x??032900
tbreg_response[3] = 0x????00ec

4.16 Lamp Test (0 x 00ee)

This diagnostic command initiates the same lamp test sequence that occurs during power-on reset. There is no response. The yellow *ACQ* and green *SYNC* panel lights are illuminated briefly, one at a time. The In-Sync output on the *TIMING* connector will be asserted while the green *SYNC* panel light is illuminated. Write command 0x000000ee to tbreg_cmd[3].

4.17 Blink Yellow Mode (0 x 00b0 and 0 x 00b1)

This diagnostic command blinks the yellow *ACQ* panel light briefly each time the board *finishes* processing *any* command. If the *ACQ* indicator is already lighted, it will extinguish briefly when a command is processed. This can be helpful during software debugging. This mode is disabled when a power-on reset or Forced Reset occurs. There is no response.

Write 0x000000b1 (enable) or 0x000000b0 (disable) to tbreg_cmd[3].

NOTE: This command can also be used to provide a visual cue. For example, the user software can be written to send the enable command, immediately followed by a disable command, when a time tag event is detected, or when the interrupt handler routine is entered, or when an external device is ready, etc.

5 Driver Support

Please contact your sales representative for information about Spectracom's bus-level timing board driver support for Windows, Linux, VxWorks, and a variety of other platforms. You may also visit our website at www.spectracomcorp.com to download datasheets and manuals.

REVISION HISTORY

Revision Level	*ECN Number*	*Description*
B	**—**	First conversion of legacy KSI documentation to Spectracom documentation.
C	**2022**	Corrected errors in Phase Noise values. Made minor style and format changes.
D	**2218**	Changed lower limit of IRIG-B input voltage range to 3.6V.
E	**2295**	Corrections to various IRIG-A and IRIG-B specifications.

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